Ordering number : ENA1919

LV0223CV

Monolithic Linear IC

Front Monitor OE-IC for Optical Pickups

ON Semiconductor®

http://onsemi.com

Overview

The LV0223CV is a front monitor optoelectronic IC for optical pickups that has a built-in photo diode compatible with three waveforms. LV0223CV is small size and type CSP packages.

Functions

- PIN photodiode compatible with three wavelengths incorporated.
- Gain adjustment (-6dB to +6dB in 256 steps) through serial communication.
- Amplifier to amplify differential output.

Specifications

Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC}		6	V
Allowable power dissipation	Pd	Glass epoxy both-side substrate 55mm × 45mm × 1.6mm Copper foil area (head: about 90% Tail: about 90%), Ta=75°C	143	mW
Operating temperature	Topr		-20 to +75	°C
Storage temperature	Tstg		-40 to +100	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Operating supply voltage	V_{CC}		4.5	5	5.5	V
Output load capacitance	C_O		12	20	33	pF
Output load resistance	Z_O		3			kΩ

Electrical Characteristics at Ta = 25°C, V_{CC} = 5V, RL=6kΩ, CL=20pF

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Current dissipation	I_{CC}		13.3	17	22.1	mA
Sleep current	Islp				0.6	mA
Output voltage when shielded	V_C	At shielding	1.85	2.0	2.15	V
Output offset voltage	Vofs	At shielding, voltage between VOP-VON	-30	0	30	mV
Temperature dependence of offset voltage *1	Vofs	Ta=-10 to +75˚C	-60	0	60	μV/˚C
Optical output voltage *1 Voltage between VOP-VON	VLC	Low Gain, λ=780nm, G=0dB	0.21	0.262	0.31	mV/μW
	VLD	Low Gain, λ=650nm, G=0dB	0.22	0.275	0.33	mV/μW
	VLB	Low Gain, λ=405nm, G=0dB	0.14	0.172	0.21	mV/μW
	VM1C	Middle1 Gain, λ=780nm, G=0dB	0.66	0.83	0.99	mV/μW
	VM1D	Middle1 Gain, λ=650nm, G=0dB	0.70	0.87	1.05	mV/μW
	VM1B	Middle1 Gain, λ=405nm, G=0dB	0.43	0.54	0.65	mV/μW
	VM2C	Middle2 Gain, λ=780nm, G=0dB	1.97	2.46	2.95	mV/μW
	VM2D	Middle2 Gain, λ=650nm, G=0dB	2.07	2.58	3.10	mV/μW
	VM2B	Middle2 Gain, λ=405nm, G=0dB	1.29	1.62	1.94	mV/μW
	VH1C	High1 Gain, λ=780nm, G=0dB	3.35	4.19	5.02	mV/μW
	VH1D	High1 Gain, λ=650nm, G=0dB	3.52	4.40	5.28	mV/μW
	VH1B	High1 Gain, λ=405nm, G=0dB	2.20	2.75	3.30	mV/μW
	VH2C	High2 Gain, λ=780nm, G=0dB	5.72	7.15	8.58	mV/μW
	VH2D	High2 Gain, λ=650nm, G=0dB	6.02	7.52	9.02	mV/μW
	VH2B	High2 Gain, λ=405nm, G=0dB	3.76	4.70	5.64	mV/μW
Light output voltage adjustment range *1	G	G=0dB reference, absolute value of adjustment width	5.5	6.0	6.5	dB
D range *1	VoD	Voltage between VOP-VON	1700	2200		mV
Frequency characteristics *1, *2	FcC	-3dB(1MHz reference), λ=780nm Light input = 40μW(DC) + 20μW(AC)	60	80		MHz
	FcD1	-3dB(1MHz reference), λ=650nm Light input = 40μW(DC) + 20μW(AC) Low/Middle1/2 Gain	60	85		MHz
	FcD2	-3dB(1MHz reference), λ=650nm Light input = 40μW(DC) + 20μW(AC) High1/2 Gain	60	80		MHz
	FcB1	-3dB(1MHz reference), λ=405nm Light input = 40μW(DC) + 20μW(AC) Low/Middle1/2 Gain	60	85		MHz
	FcB2	-3dB(1MHz reference), λ=405nm Light input = 40μW(DC) + 20μW(AC) High1/2 Gain	60	80		MHz
Settling time *1	Tset			10	15	ns
Response time *1	Tr, Tf	Vo=0.9Vp-p, output level 10 to 90% fc=10MHz, duty=50%		4	10	ns
Overshoot *1	Ovst	Vo=0.9Vp-p, G=0dB			15	%
Undershoot *1	Unst	Vo=0.9Vp-p, G=0dB			15	%
Linearity *1	Lin	At output voltage 0.5V and 1.0V (Between VOP-VON)	-1	0	1	%
Light-output voltage temperature dependence Voltage between VOP-VON *1, *3	TC	λ=780nm, 25˚C reference	7	10	13	%
	TD	λ=650nm, 25˚C reference	-1	2	5	%
	TB	λ=405nm, 25˚C reference	-1	2	5	%

Item with *1 mark indicate the design reference value.

Item with *2 mark indicate the frequency characteristics when VOP and VON are applied individually.

The frequency characteristics are for the output voltage adjustment range is -6 to +6dB

Item with *3 mark indicates the temperature dependence for the case of High2 / High1 / Middle2 / Middle1 / Low gain and for the case when the temperature is 25 to 75˚C for the output voltage adjustment range of -6 to +6dB

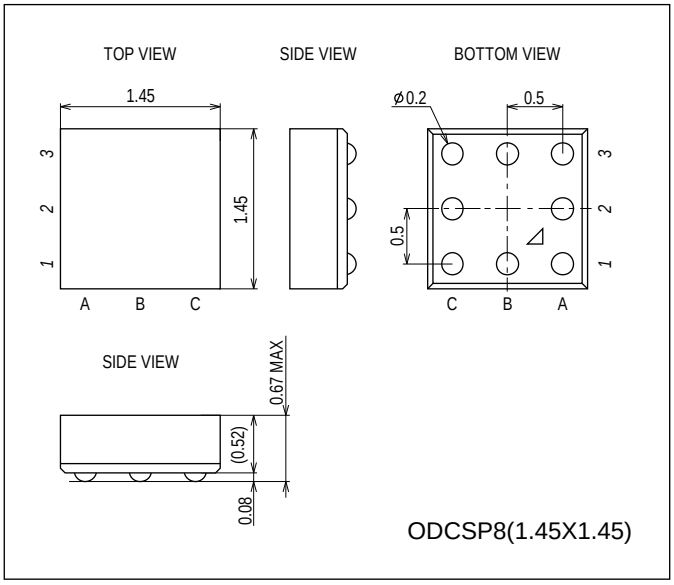
[Expression of output voltage]

V_N = (sensitivity / 2) × 5400 / (5400-16 × GCAstep) × light intensity (μW)

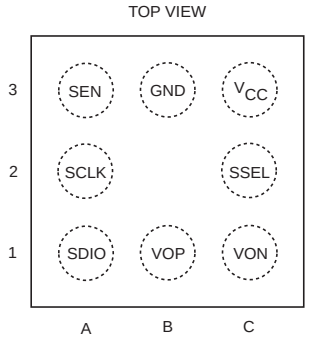
Package Dimensions

unit : mm (typ)

3407

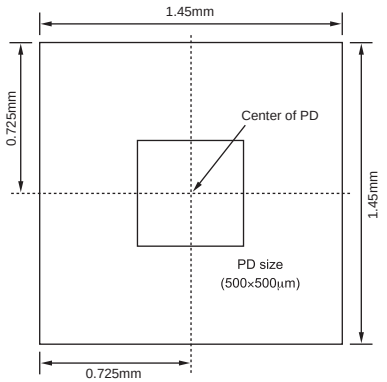


Pin Assignment



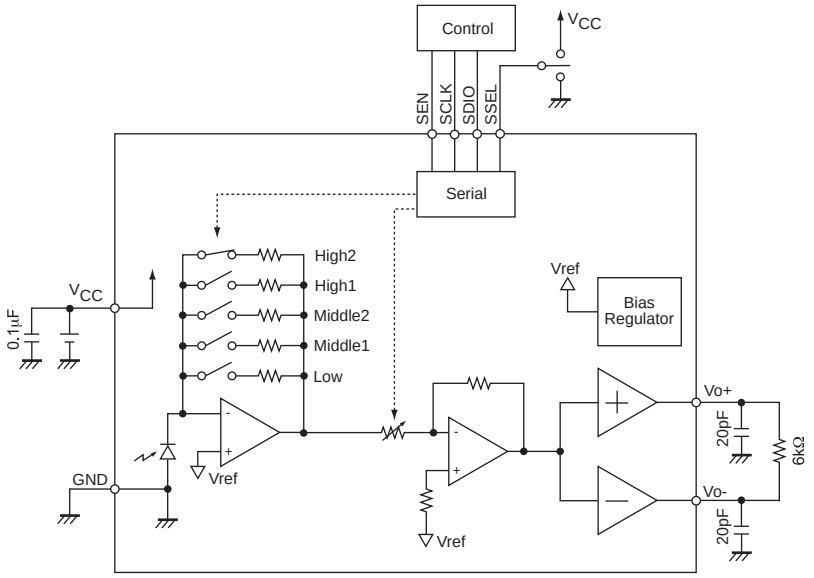
Pin No.	Pin name	Function
1A	SDIO	Serial communication Data pin
1B	VOP	Positive side output pin
1C	VON	Negative side output pin
2A	SCLK	Serial communication Clock pin
2C	SSEL	Register selection pin
		SSEL = Low : Address 00 to 0Fh used
		SSEL = High : Address 10 to 1Fh used
		SSEL = Open : Address 70 to 7Fh used
3A	SEN	Serial communication Enable pin
3B	GND	GND pin
3C	V_{CC}	Power supply voltage pin

PD assignment



*PD size for reference to be used for design

Block diagram and Test circuit diagram



Resister table

Enable selection of the register group from the SSEL pin.

SSEL = Low

	Address	7	6	5	4	3	2	1	0
Name	00h	**POWER**		**IV GAIN SEL**		**GAIN SEL**		**IV GAIN2**	
Default		00		00		00		1	0
Value		11: Power on 00/01/10: Sleep		*4		00/01: BD 10: DVD 11: CD		*4	
Name	01h	**BD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	02h	**DVD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	03h	**CD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	0Eh	**TEST1 (*1)**							
Name	0Fh	**TEST2 (*1)**							

SSEL = High

	Address	7	6	5	4	3	2	1	0
Name	10h	**POWER**		**IV GAIN SEL**		**GAIN SEL**		**IV GAIN2**	
Default		00		00		00		1	0
Value		11: Power on 00/01/10: Sleep		*4		00/01: BD 10: DVD 11: CD		*4	
Name	11h	**BD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	12h	**DVD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	13h	**CD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	1Eh	**TEST1 (*1)**							
Name	1Fh	**TEST2 (*1)**							

Continued on next page.

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SSEL = Open

	Address	7	6	5	4	3	2	1	0
Name	70h	**POWER**		**IV GAIN SEL**		**GAIN SEL**		**IV GAIN2**	
Default		00		00		00		1	0
Value		11: Power on 00/01/10: Sleep		*4		00/01: BD 10: DVD 11: CD		*4	
Name	71h	**BD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	72h	**DVD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	73h	**CD GAIN**							
Default		1	1	1	1	1	1	1	1
Value		00000000 to 11111111							
Name	7Eh	**TEST1 (*1)**							
Name	7Fh	**TEST2 (*1)**							

*1 TEST1 and TEST2 are either the time when power is applied or “00000000” is set. Do not attempt to change “00000000” during operation.
“00000000” is returned when reading is made.

*2 No problem in terms of operation occurs even when writing is made to the address 04h to 0Dh and 14h to 1Dh and 74h to 7Dh.
“00000000” is returned when this address is read.

*3 When I performed address reading except the register group set by an SSEL terminal, I keep Hi-Z without paying a value.

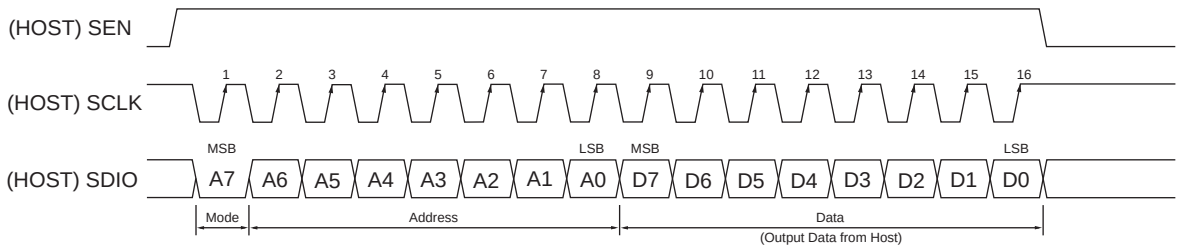
*4 Please set the gain setting of the I/V amplifier referring to the table below.

I/V amplifier gain setting table

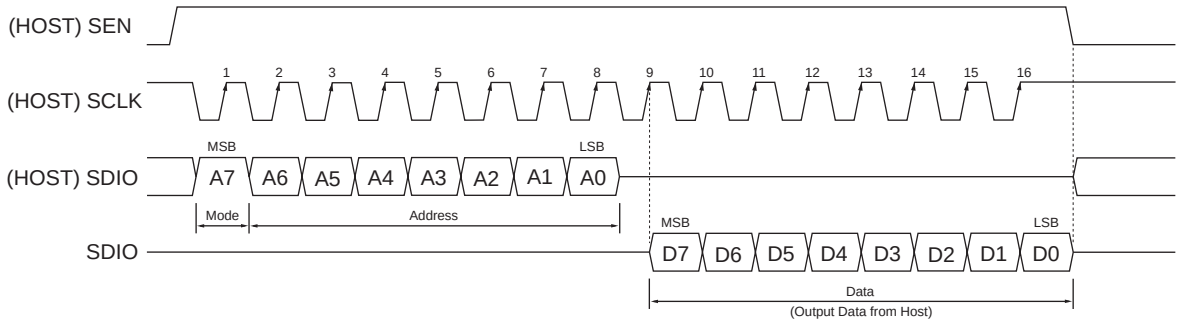
00h/10h/70h		5	4	1
Name		**IV GAIN1 SET**		**IV GAIN2**
Default		00		1
IV GAIN	High2	00/01		1
	High1	10/11		1
	Middle2	00/01		0
	Middle1	10		0
	Low	11		0

Serial protocol

WRITE timing chart



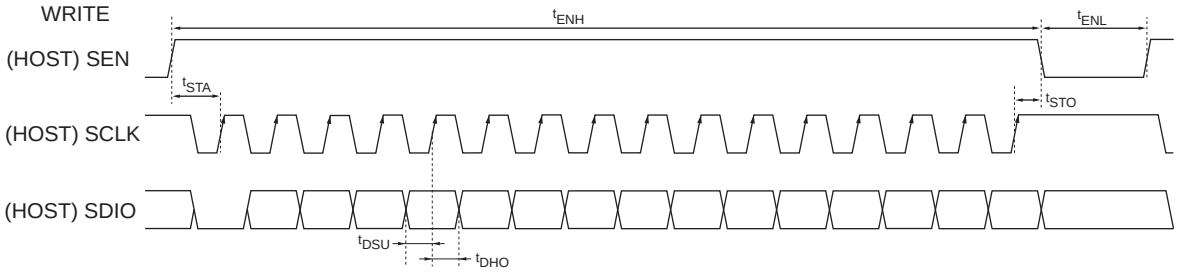
READ timing chart



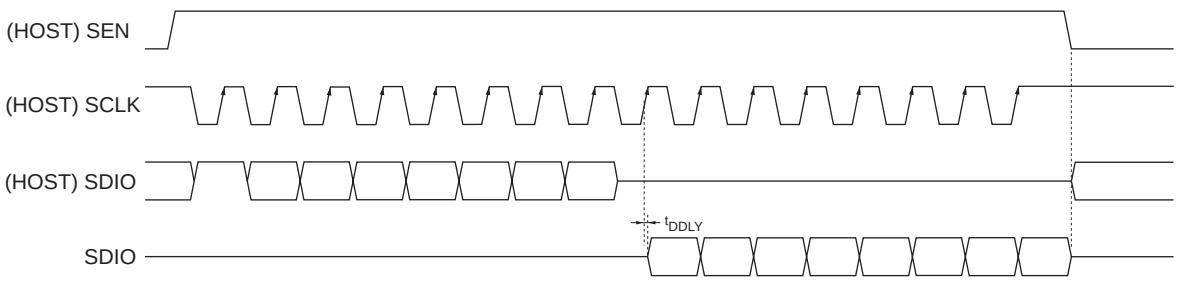
SDIO pin load / CL=20pF (The table below shows the design reference value.)

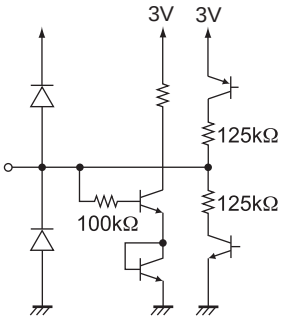
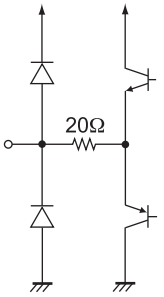
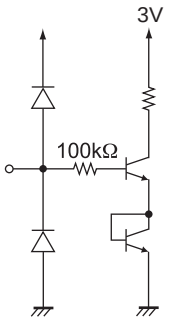
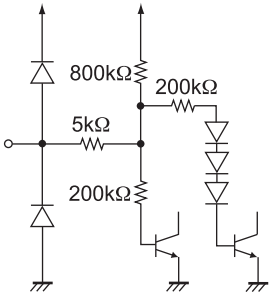
Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency Write	f_{SCL}	0		10	MHz
SCL clock frequency Read	f_{SCL}	0		4	MHz
SDIO data setup time	t_{DSU}	50			ns
SDIO data hold time	t_{DHO}	50			ns
SDIO output delay	t_{DDLY}		10	80	ns
SEN “H” period	t_{ENH}	1.6			µs
SEN “L” period	t_{ENL}	200			ns
SCL rise time after SEN rise	t_{STA}	60			ns
SEN fall time after final SCL rise	t_{STO}	100			ns
Serial input “H” voltage	V_IH	2.4		3.7	V
Serial input “L” voltage	V_IL			0.6	V
SDIO output “H” voltage	V_OH	2.5	2.9	3.3	V
SDIO output “L” voltage	V_OL	0	0.3	0.8	V

WRITE



READ



Pin	Type	Equivalent circuit diagram
SDIO	Input Output	
VOP VON	Output	
SCLK SEN	Input	
SSEL	Input	

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